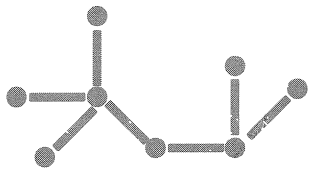

Transmission of coded sound signals in a future ATM network

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The article describes a method for the adaptation of high–quality digital sound signals to a future integrated–services broadband network. The digital signals, with a highly–reduced bit–rate, are transmitted in cells in the asynchronous transfer mode.

The method can be applied to the networking of signals for Digital Audio Broadcasting services between studio centres and the DAB transmission multiplexer.

1. Introduction

In recent years, sound coding methods have been developed which allow a substantial reduction in the data–rate compared to traditional linear coding methods. These new coding schemes are being used, for example, in Digital Audio Broadcasting (DAB), and they take advantage of the masking effects of the human ear to achieve a reduction in the redundancy. As a result of this redundancy reduction, audio decoders are highly sensitive to errors in the received digital signal.

In the case of DAB, signals from several digital coders are transmitted to a central multiplexer via serial data lines. For this purpose it is possible to use serial data transmission circuits, time–slots in multiplex systems, or modems operating on analogue lines. The integrated–services digital network (ISDN) can certainly be used also for the transmission of these digital audio signals.

In the transition to the broadband ISDN, which will operate in asynchronous transfer mode (ATM), the specific characteristics of this mode of operation must be taken into account. In an ATM network, the data–stream is structured into cells. Cell losses can occur, for example as a result of buffer over–flow during transmission or bit–errors. This implies that, unless special measures are taken to adapt the transmitted signals to the ATM network, the audio decoder will have to be able to correct the bit–errors caused by cell loss [1].

Original language: English
Manuscript received 5/4/94.

Dieser Aufsatz erscheint in Deutsch unter dem Titel "Übermittlung von codierten Audiosignalen niedriger Bitrate in einem zukünftigen ATM–Netz" in Rundfunktechnische Mitteilungen, Heft 3, 1994.

By means of a process known as "terminal adaptation", the coder/decoder can be matched to the requirements of the ATM network. This offers several advantages, including the correction of invidual cell losses. A terminal adapter is being developed in the RACE project R 2061 EXPLOIT, which will allow the adaptation of an ISO–MPEG Layer II codec [2] to an ATM network. The correction of a small number of mis–routed or lost cells is made possible by appropriate measures such as forward error–correction (FEC), the addition of redundancy bits, and subsequent interleaving during the writing of data bits into buffer matrices.

2. Sound coder

The mode of operation of the sound coder requiring adaptation to the ATM has been described elsewhere and the present *Section* will outline only

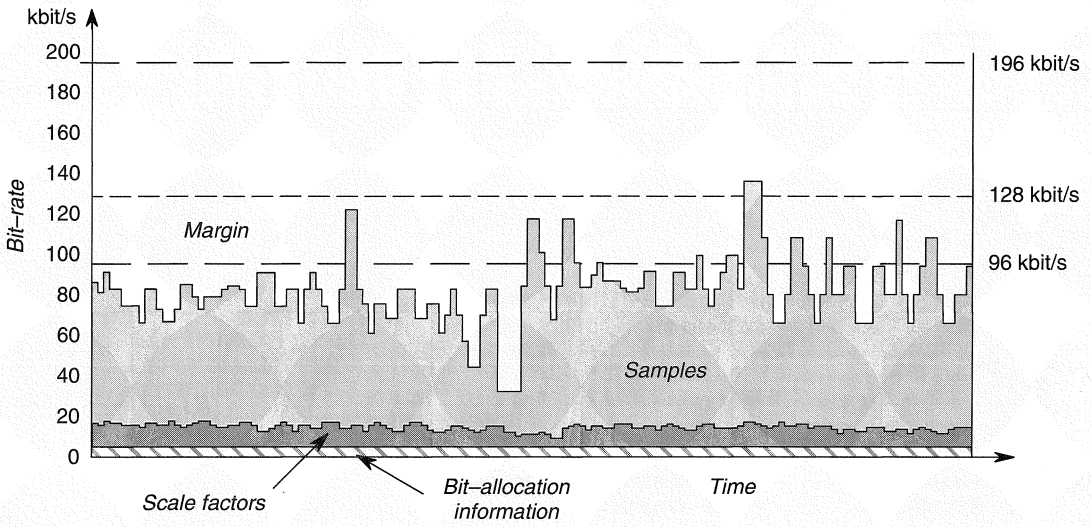


Figure 1
ISO 11172–3 Layer II multiplex signal.

those features which are necessary for an understanding of the adaptation process.

2.1. Coding process

The sound coding system makes use of the characteristics of the human ear and, in particular, the masking effect which allows a reduction in the data–rate. For a given analogue sound quality, a reduction of the bit–rate by a factor of about four can be achieved in comparison with linear coding.

Codecs operating in accordance with the ISO MPEG–2 standard are now available on the market. In addition to the point–to–point connection of coded sound signals for contribution purposes, the conveyance of signals to a DAB multiplexer will be an important requirement in the future. It is possible to adapt the bit–rate of the codec to the requirements of the user and the network. The bit–rates range from 56 kbit/s for a monophonic channel of lower quality to 384 kbit/s for a stereophonic sound channel of very high quality.

Although the bit–rate generated during the coding procedure is not constant (see *Fig. 1.*), the coder delivers a constant bit–rate at its output. The extra capacity can be used for data accompanying the programme and/or for error protection of the digital signal [3].

2.2. Transmission frames

The transmission frame for these digital sound signals is described in [4] and shown schematically in *Fig. 2*. The frame duration, for a sampling rate of 48 kHz, is 24 ms, irrespective of the output bit–rate. Frame alignment is achieved using 16 bits in the 32–bit header (*Fig. 3.*).

A further group of 16 bits is assigned to decoder control. Bits 17 to 20 and the bit–allocation bits (see *Fig. 1*) are of special importance in connection with the transmission of signals in an ATM network, because they indicate the bit–rate of the digital signal and the length of the data block in the frame.

3. Terminal adaptation

As noted earlier, terminal adaptation to the requirements of the network is necessary for digital signals which are to be transmitted in an ATM network. The generation of cells is one of the most important pre–requisites. Other requirements in-

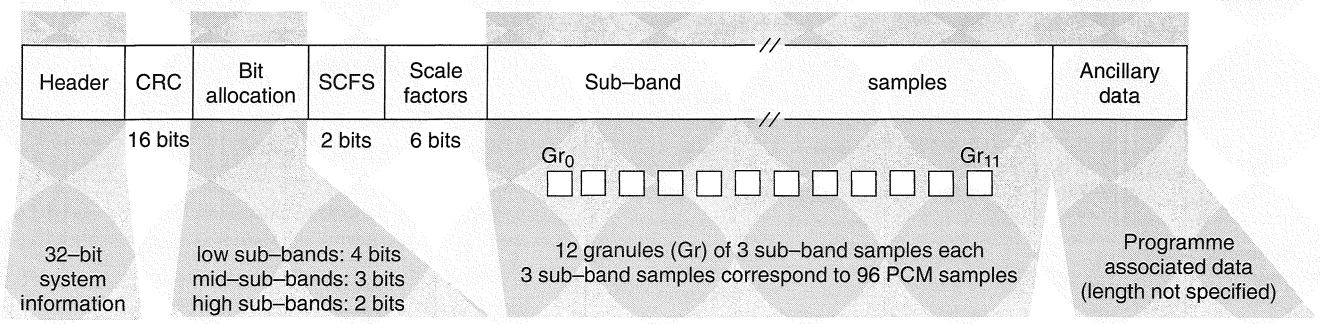


Figure 2
ISO 11172–3 Layer II frame structure.

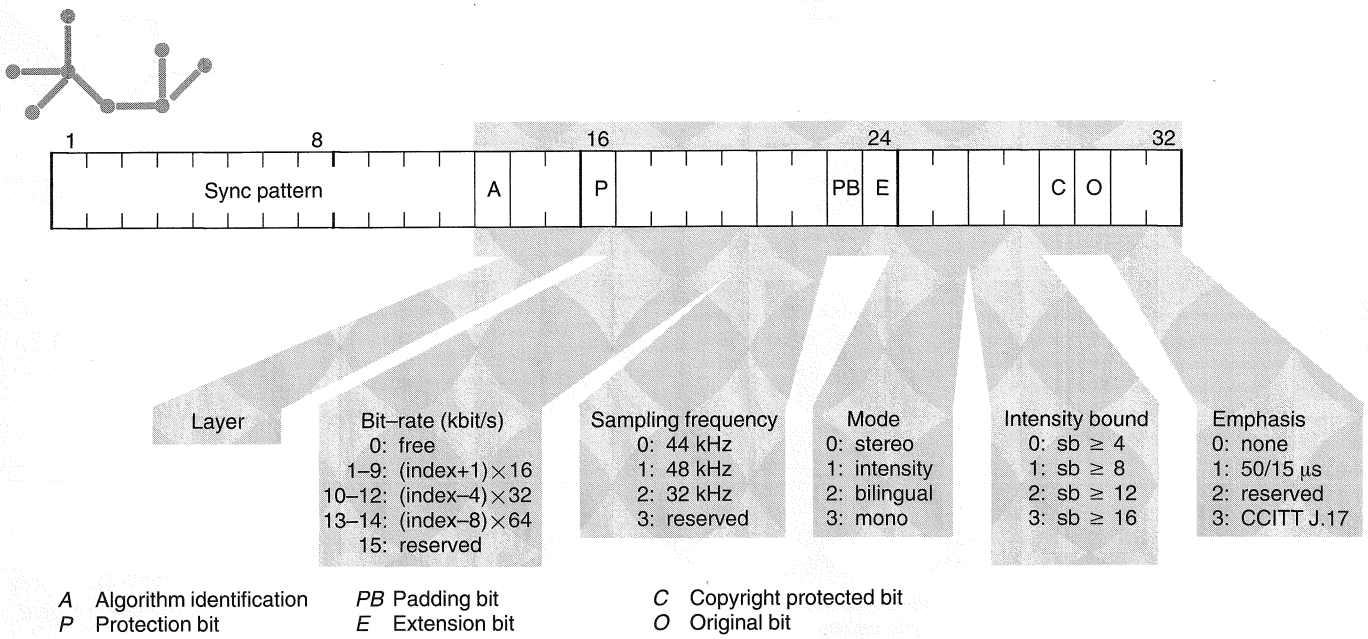


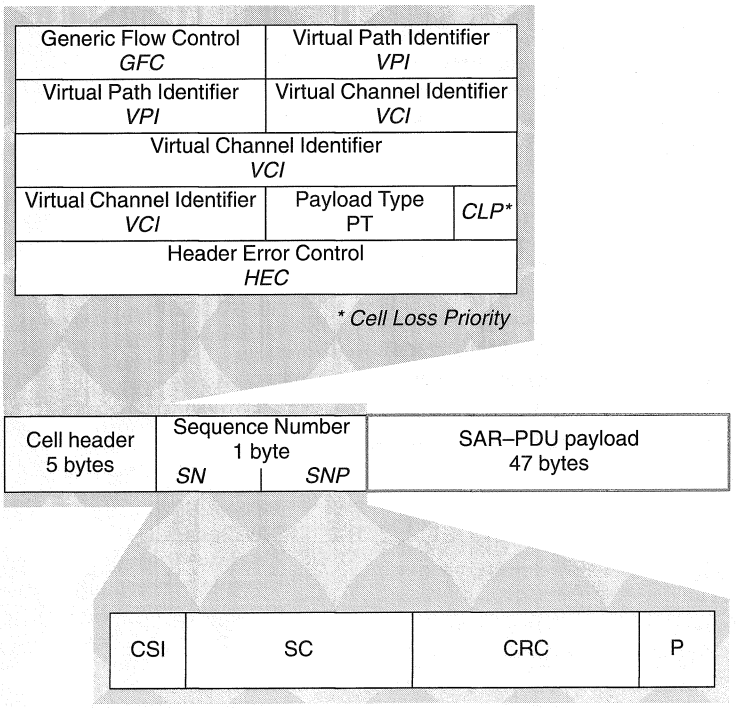
Figure 3
ISO 11172–3 Layer II multiplex header.

clude protective measures against bit errors caused by cell loss, and provision for the recovery of the signal clock from the transmitted data.

3.1. ATM adaptation layer

The present article considers only cells of class A (services of constant bit–rate, as defined in ITU–T Recommendation I.362) of the ATM Adaptation Layer (AAL) type 1, corresponding to ITU–T Recommendation I.363. The cell structure is depicted in *Fig. 4*.

Figure 4
Cell structure for AAL type 1.



SN Sequence Number
SNP Sequence number protection
CRC Cyclic Redundancy Check
CSI Convergency sub–layer indication
P Parity bit
SC Sequence Count

Every cell consists of 53 bytes, including a header composed of 5 bytes. Information controlling the transmission of the cells on a virtual path or virtual circuit are included in this header. If required, this information can be translated in the individual nodes of the ATM network. It is necessary, as a minimum requirement, to make a distinction between cells which carry signalling from and to the controller, and user cells which carry user data.

The remaining 48 bytes are reserved as transmission capacity. In the AAL type 1, which it is planned to use for sound transmission, the first byte of the information field is responsible for the consecutive numbering of the cells at the transmitter and for the transmission of these numbers to the receiver. The sequence count (SC), from 1 to 7, are transmitted in bits 6 to 11. This makes it easy to detect a fault in the sequence of cells at the receiving end, because the cell sequence is not deliberately changed during transmission in the ATM network and changes can occur only if there is cell loss caused by buffer over–flow. Cell loss can therefore be detected immediately.

The first bit (CSI) marks the beginning of an interleaving matrix assigned to the convergence sub–layer (CS). The remaining four bits are used to protect the sequence number against errors.

3.2. Interleaving and error correction

Cell loss can occur during the transmission of digital signals in an ATM, although the probability of such losses is very low. The buffers used in ATM networks are dimensioned in such a way that there will be no buffer over–flow for certain statistical distributions of the traffic volume leaving the signal sources. The policing function that is provided

only monitors the situation of an individual source, and it restricts the maximum data volume of that source. If the maximum data volume from several sources is attained at the same time, however, the buffer will overflow and cell loss will occur. Cell loss, or mis–insertions due to the mis–routing of cells after bit–errors in the header, are rare.

The correction of errors due to cell losses is one of the main tasks of the terminal adapter. In this context, the coding of signals with the help of a code which allows the correction of errors and the subsequent interleaving of data bits at the transmitting end, is a suitable method. At the receiving end, cell losses (i.e. the absence of entire data blocks, depending on the length of the data field) are reduced to individual errors during the de–interleaving process.

In the present case, in which the data transmission takes place with a low bit–rate, the insertion of an additional parity bit into the n data bits (e.g. $n = 7$), and the subsequent bit–wise interleaving in one block of $(n + 1) \times 376$ bits is sufficient (see *Fig. 5*). Cell losses are detected in the receiver as a result of the missing sequence numbers. If a cell loss is detected, 376 dummy bits are substituted for the information that was expected in the information field; the dummy bits are processed as if they were part of the received signal but are marked as being incorrect bits. In the bit–stream obtained after de–interleaving, the loss of a data block having a length of 376 bits (one information field) is converted to a series of single errors in each of 376 blocks of 8 bits. These errors can be corrected by means of the parity check, since the incorrect bits are all marked. The parity bit is compared with the parity bit generated at the transmitter; if the two

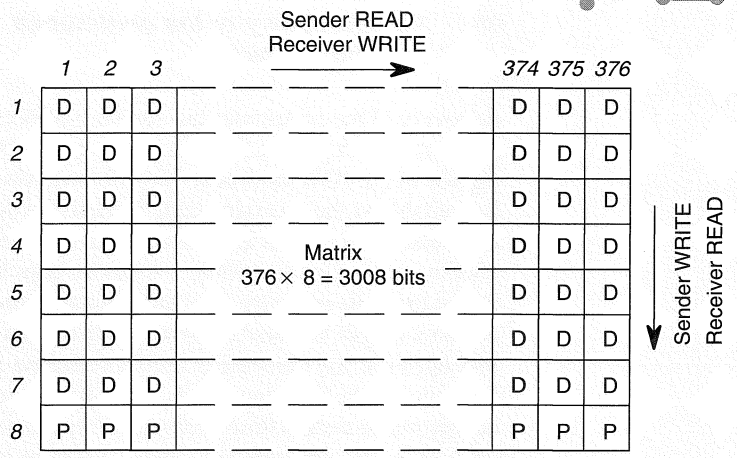
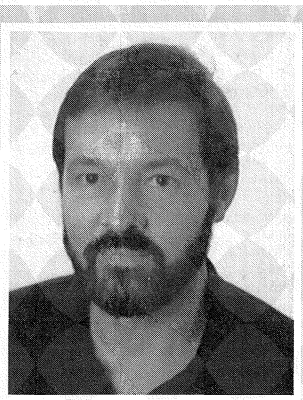


Figure 5
Interleaving matrix.

parity bits are the same then the bit at the marked position is correct, whereas if the parity bits are different, the marked bit must be inverted.

The data rate in this application is low enough to ensure that only individual cells can get lost [5], so the proposed procedure for protection against cell loss is sufficient. However, the procedure cannot be applied if there is cell loss *and* an additional bit error within a block of eight cells. Assuming a bit–error ratio (BER) of 10^{-6}, and a cell–loss ratio (CLR) of 10^{-8} for individual bit–errors, the probability of coincidence of the two events is BECLR = 2.1×10^{-10}. If the duration of a data block is T_B = 6.85 ms (for a data–rate of 384 kbit/s), error–coincidence occurs at a mean interval of $T_D = 3.4 \times 10^7$ s, corresponding to 396 days. Even if the CLR is increased to 10^{-6}, for the same BER, the mean interval would still be 3.9 days. It should also be borne in mind that coincidence of the two errors in an interleaving block only results in one or two bit errors.



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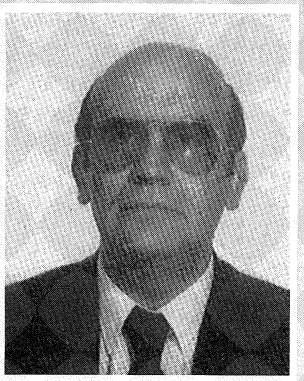

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3.3 Recovery of the continuous bit–stream

Recovery of the continuous bit–stream is a special problem with regard to the transmission of digital signals in the ATM network. No reference clock is available at the receiving end, because the data are transmitted in cells and therefore do not arrive continuously. Another problem is that the gaps between the cells of a virtual connection are not of constant length, because the source data are stored in a buffer at the transmitter until a complete information field has been filled. The cell can only be released at certain time intervals, to replace idle cells in the transmitted cell stream, so there is a variable waiting time. Furthermore, the cells are subject to variable delays in the network exchanges, since free time positions must be found in the out–going direction with the result that cells have to remain in the buffer for different periods of time. All these factors cause a considerable variation of cell delay, known as variable cell delay.

It is necessary to recover a continuous data stream corresponding to the original one, from this very dis–continuous data–stream, without incurring data loss. This is quite easy by applying an adaptive method of clock recovery. The technique uses a buffer (already needed to avoid information loss) to control a clock oscillator. If a low–pass filter with a sufficiently low cut–off frequency (in the mHz range) is assigned to the control loop, a digital signal with a very low–frequency clock jitter is obtained and this can easily be processed in the terminal.

4. Functions of the terminal adapters

The up–stream and down–stream terminal adapters have different functions, as illustrated in *Figs. 6* and *7*.

4.1. Up–stream (transmit) adapter

The transmitting terminal adapter (*Fig. 6*) is composed of the following components: parity encoder, bit–interleaver, clock oscillator and cell assembler (which, together, form the information field processor) and the line termination which establishes the connection to the network.

The tasks of the parity encoder and bit interleaver have been explained in *Section 3.2*.

The cell assembler [6] assembles the information originated by a constant bit–rate source into the cell information field, inserts the sequence number in the first byte of the information field and appends the header to form a complete cell at the output. The basic functions of the cell assembler are:

- serial–to–parallel conversion;
- assembly of data to form the information field;
- sequence number insertion in the first byte of the information field;
- header insertion to form the complete cell;
- insertion of channel identification number (8 bits) in the third byte of the header;
- insertion of idle cells to generate a continuous cell–stream at the output.

Internally, the cell assembler comprises the following main blocks: serial–to–parallel converter, cell buffer (first–in, first–out – FIFO), sequence number/sequence number protection generator, header inserter, idle cell generator, up/down byte counter and controller.

The cell assembler takes a serial data–stream at the input. The information at the input can be at a constant bit–rate or can arrive in bursts; it is validated by the VD2 "valid data" flag. The matrix start signal indicates the beginning of the bit interleaving matrix; it will be mapped into the CSI bit of the byte containing the sequence number. After

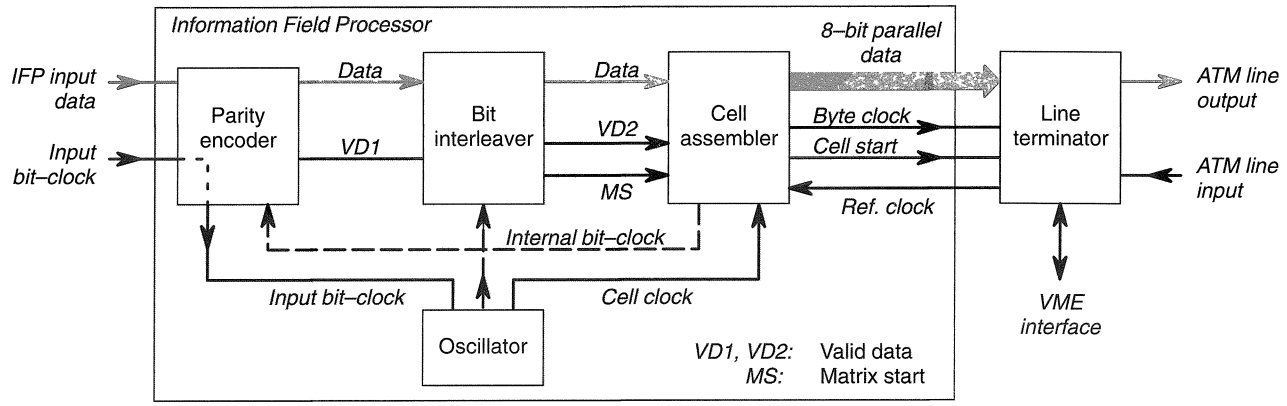


Figure 6
Audio signal Terminal Adapter – upstream.

the 47 bytes of user data and one byte sequence number have been assembled, the 5–byte header is added to form the complete cell. The third byte, carrying the channel identification number (CIN), will be be recovered by the down–stream (receiving) adapter in its original form in order to ensure that the cell stream can be assigned to the correct outputs in the terminal adapter. The output of the cell assembler is a parallel ATM interface signal. An idle cell generator inserts idle cells when there are no assigned cells waiting to be transmitted.

The line termination component adapts the ATM data–stream to the physical characteristics of the network, e.g. electrical or optical interface. The header is produced in accordance with ITU–T Recommendation I.361, with the channel identification number being translated into the virtual path or virtual channel identifier. The VME bus in the line termination offers the possibility of inserting signalling cells into the cell–stream, by the replacement of idle cells. Cells intended for use by the terminal adapter controller can be selected from the cell stream received at the up–stream terminal adapter. The network clock is recovered from the incoming bit–stream and made available to the information field processor as a reference clock.

4.2. Down–stream (receive) adapter

The down–stream terminal adapter is shown in *Fig. 7*. It also has a line terminator component for connection to the network, where the cell headers are translated and the cell–stream is split into data for the information field processor, the controller and data from idle cells. The network clock is again recovered from the incoming bit–stream and used to derive the byte clock.

The cell dis–assembler [7] is used to dis–assemble the ATM cells of constant bit–rate services. It is assumed that this component is used after the terminator, where the virtual channel identifier is translated into a channel identification number and any cells received with error are discarded. The basic functions of the cell dis–assembler are:

- cell header extraction;
- idle cell extraction;
- cell filtering based on the channel identification number;
- sequence number checking;
- handling of cell loss or insertion;
- sequence number extraction;
- dis–assembly of user data;
- parallel–to–serial conversion;
- generation of the matrix start flag;
- rate adaptation;
- partial compensation of variable cell delay;
- indication of cell losses and insertions.

Internally, the cell dis–assembler comprises the following main blocks: serial–to–parallel converter, cell buffer (FIFO), sequence number/sequence number protection processor, header extracter, channel identification number comparator, and controller. The inputs to the dis–assembler are an extended parallel ATM interface with 8–bit data, the cell start signal, a byte clock and a "valid cell" flag.

As the cell dis–assembler is connected directly to the terminator, it has to work at the full speed of 19.44 Mbyte/s and it has to remove the idle cells and filter the received cells on the basis of the cell validity flag. A comparator checks the third byte of the header, looking for the correct channel identification number. The idle cells and any cells with a wrong channel identification number are discarded. Cells which match the programme channel identification number are stored in a first–in,

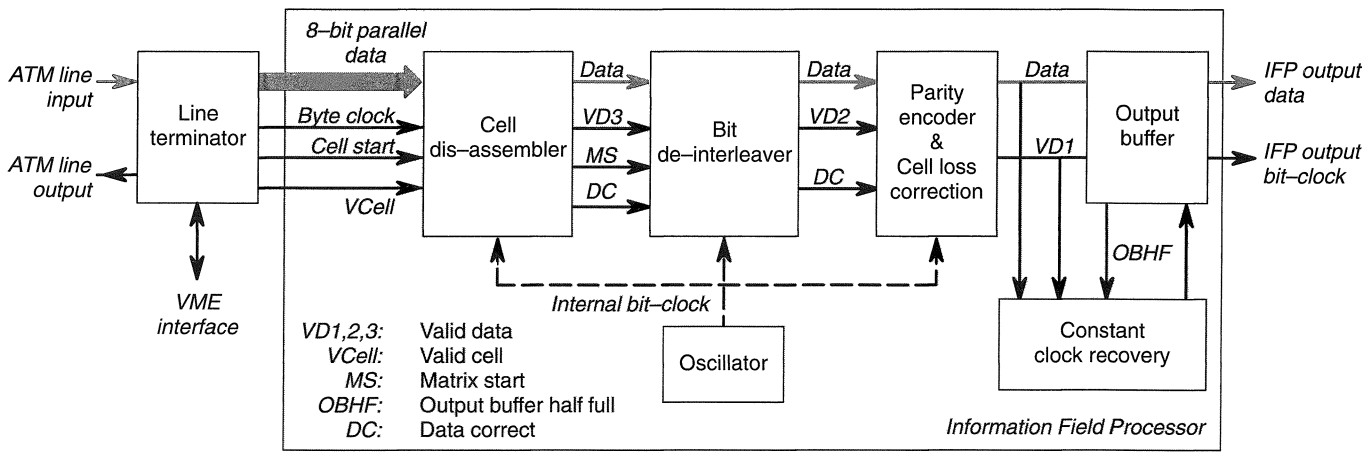
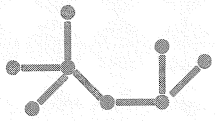


Figure 7
Audio signal Terminal Adapter – down–stream.



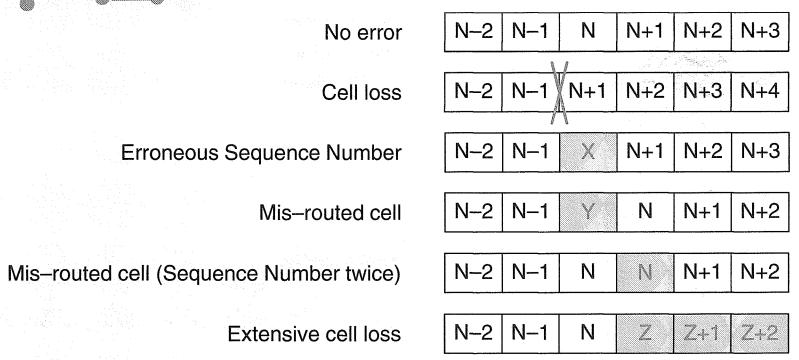


Figure 8
Possible cell errors.

first–out register. The sequence number/sequence number protection block is responsible for the detection and correction of the cells which are received out of order (*Fig. 8*). The sequence number is checked to verify that the sequence numbering is correct.

If a cell loss is detected, a dummy cell is generated and inserted into the information stream. If an inserted cell (i.e. a cell which does not belong to the wanted signal) is detected, it is discarded. If a cell with number N is missing, the lost cell is replaced by one with a pre–defined or dummy content. If, between cell N–1 and N+1, a cell with sequence number X is received, it is likely that the sequence number has been corrupted from N to X and the cell is considered to be correct. If, between cells N–1 and N, a cell with sequence number Y is received, this cell is considered as an inserted cell and is discarded. If two cells with the same sequence number N are received one after the other, there is an equal probability of one of them being the correct cell. To save memory, and to simplify the controller, the first cell is chosen as the correct cell. If a sequence of cells with sequence numbers Z, Z+1, etc. is received instead of a correct sequence with numbers N+1, N+2, etc. it is assumed that an extensive loss has occurred. If the gap between N and Z is not greater than four, dummy cells with sequence numbers in the interval N to Z are inserted and the sequence is expected to continue from Z+1. If the difference between N and Z is greater than four, the component will be re–initialised.

The matrix start signal marking the beginning of the interleaving block is recovered from the first bit of the first byte.

The bit de–interleaving block de–interleaves the data–stream. Blocks of 376 bits which contain errors as a result of cell loss are reduced to individual bit errors in blocks of eight bits each; the errors are corrected in the parity decoder/cell–loss corrector. To complete the system, there is an output buffer with a storage capacity of three cells [8]. This buffer is necessary to compensate for severe short–term timing irregularities of the cell sequence, caused by the variable cell delay.

The clocks required in the information field processor are made available by clock recovery. The frequency of the clock oscillator in the recovery sub–system is controlled by the filling level of the output buffer.

5. Conclusion

A special form of adaptation, known as terminal adaptation, is needed for the transmission of low–bit–rate digital sound signals of high quality in the ATM network. This adaptation is currently being investigated within the framework of the RACE Project R 2061 EXPLOIT. The terminal adapter characteristics will be tested and integrated in the RACE 2061 EXPLOIT test–bed.

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